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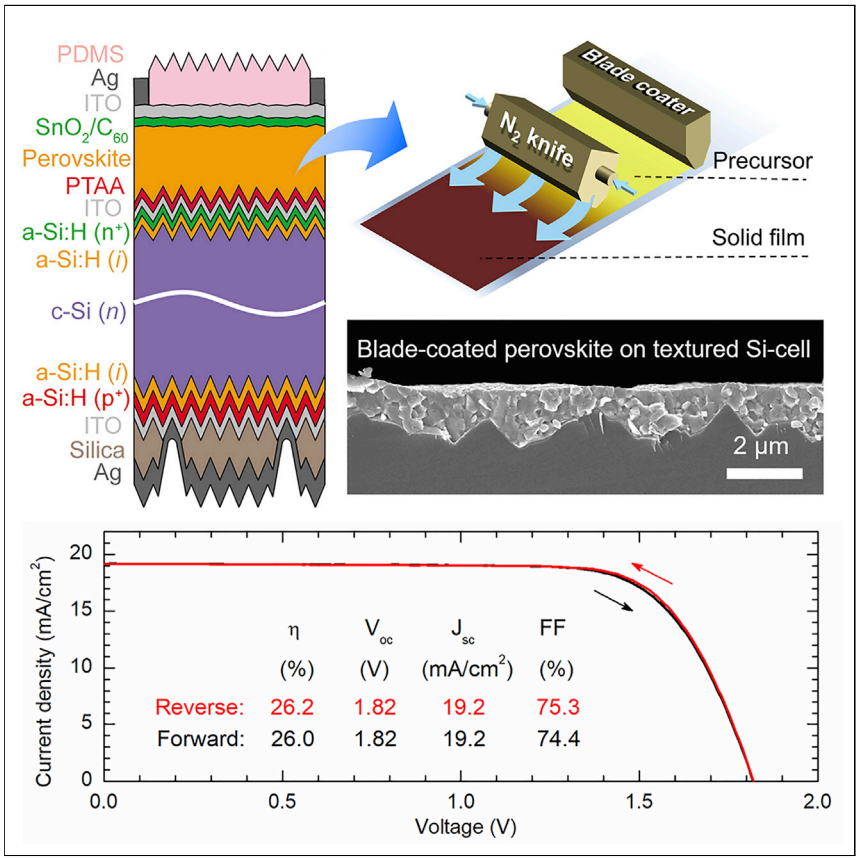

A new monolithic perovskite/silicon tandem solar cell architecture is proposed based on double-side-textured silicon cells with sub-micrometer pyramids. These pyramids are rough enough to scatter light within silicon nearly as efficiently as large pyramids but smooth enough to solution process a perovskite film. A blade-coated perovskite film planarizes the textured silicon cell. With a textured light-scattering layer added to the top to reduce front-surface reflectance, a monolithic perovskite/silicon tandem cell reaches an efficiency of 26%.

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HIGHLIGHTS

A new tandem architecture enabled by silicon cells with sub-micrometer texture

Deposition of perovskites on double-side-textured silicon by scalable blade coating

Perovskite with thickness greater than pyramid height planarizes the textured silicon

26%-efficient monolithic perovskite/silicon tandem device

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Blade-Coated Perovskites on Textured Silicon for 26%-Efficient Monolithic Perovskite/Silicon Tandem Solar Cells

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SUMMARY

Integrating perovskites onto textured silicon provides a pathway to 30% tandem solar cells. However, deposition of 0.5–1 μm thick perovskite layers from solution onto textured silicon with typical pyramid heights of 3–10 μm remains a challenge. We propose a new tandem architecture that enables scalable, solution-based blading of perovskites onto silicon wafers textured with pyramids less than 1 μm in height. These pyramids are rough enough to scatter light within the silicon nearly as efficiently as large pyramids but smooth enough to solution-process a perovskite film. A nitrogen-assisted blading process deposits both a conformal hole transport layer and a planarizing perovskite layer that fully covers the textured silicon, at a speed of 1.5 m/min. With a textured light-scattering layer added to the top of the tandem to reduce front-surface reflectance, we achieve a perovskite/silicon tandem cell with an efficiency of 26% on textured silicon.

INTRODUCTION

Perovskite/silicon tandem solar cells have the potential to break the single-junction efficiency limit of silicon cells and further drive down the cost of silicon photovoltaics.[1–3] Tremendous progress has been made in the past 5 years in the development of efficient perovskite/silicon tandem devices, primarily fabricated on single-side-polished silicon cells.[4–12] With this architecture and an anti-reflection layer or light-scattering layer, several groups have reported tandem devices with efficiencies over 25%.[8–12] For example, Chen et al. reported a 25.4%-efficient tandem with a magnesium fluoride (MgF_2) anti-reflection layer;[8] Bush et al. reported a 25.0%-efficient tandem with a textured polydimethylsiloxane (PDMS) light-scattering layer;[9] and Jost et al. reported a 25.5%-efficient tandem with a similar textured light-scattering foil.[10] In these devices, the flat silicon surface facilitates deposition of perovskite films from solution, but the high front-surface reflectance and inability to scatter light into the silicon bottom cell reduce the photogenerated current in the sub-cells and thus the tandem device efficiency. For example, even with an anti-reflection layer or light-scattering layers, the three high-efficiency cells reported above suffered reflection losses of 4.8, 3.2, and 2.5 mA/cm^2, respectively,[8–10] and the light-scattering layers were shown not to provide the light trapping afforded by a double-side-textured silicon cell.[13] Moreover, perovskite/silicon tandem solar cells that rely on a polished wafer surface are likely to face significant cost barriers because industrial silicon wafers are typically etched and textured on both sides, and chemical-mechanical polishing is cost prohibitive.[14]

Context & Scale

As an outstanding tandem partner for silicon solar cells, solution-processed metal halide perovskites offer highly efficient photovoltaics at low cost. To date, the reported monolithic perovskite/silicon tandem cells are fabricated primarily on silicon cells with a front-side-polished surface, which is not compatible with the industrial-standard double-side-textured silicon cells. Thermal evaporation of perovskite film has been reported for perovskite/silicon tandem cells on textured silicon to bridge the gap, but it sacrifices the advantage of solution-processed perovskites. Here, we develop a new tandem architecture that enables scalable, solution-based blading of perovskites onto textured silicon wafers. This new tandem architecture combines the advances of textured silicon photovoltaics and solution-processed perovskite photovoltaics to increase the efficiency while reducing the cost of monolithic perovskite/silicon tandem cells.

Textured monocrystalline silicon wafers, to which the solar industry is rapidly transitioning,[15] have pyramidal texture with a typical size of 3–10 μm on both surfaces, formed naturally by anisotropic etching in alkaline solutions.[16] The random pyramidal texture can reduce the AM1.5G-weighted front-surface reflectance of silicon wafers to <12% and to <2% with an anti-reflection coating.[16] In addition, wafers with random pyramidal texture have been demonstrated to achieve light absorption close to that of the Lambertian limit.[17,18] It is thus important to deposit perovskites on textured silicon to both pave the way to manufacturing and achieve the full efficiency potential of perovskite/silicon tandems. However, the thickness of perovskite films in optimized perovskite solar cells is typically 0.5–1 μm, due in part to the limited diffusion length of polycrystalline perovskite films.[19–24] As this is much thinner than the standard pyramid height, such perovskite layers must be conformally deposited to avoid shunting.

Thermal evaporation, whether alone or in combination with other processing steps, has recently been reported as one approach to conformally coat perovskite absorbers on textured silicon.[25] A two-step process was reported by Sahli et al. to deposit perovskite films on textured silicon solar cells with a pyramid height of approximately 5 μm.[25] Conformal coating of mixed CsBr and PbI_2 was first achieved by thermal co-evaporation, and then a mixed FABr and FAI solution was spun on the evaporated films, followed by thermal annealing, to obtain conformal perovskite films. The reduced reflection loss from the textured surface enabled a tandem with only 1.64 mA/cm^2 reflection loss and 25.2% efficiency.[25] Several groups have successfully developed one-step vacuum deposition processes for complex compositions of perovskite films,[26–32] as is necessary for high-efficiency wide-band-gap perovskite solar cells that commonly have both mixed cations and mixed halides.[33–35] However, there are many remaining challenges: these perovskite compositions require four or more precursor sources, creating a complex processing space; evaporation tools require high capital expenses and have not successfully been introduced to the photovoltaics market at scale; and vacuum-deposited perovskites have not yet achieved the same cell efficiencies as their solution-processed counterparts.[32] The last challenge is exacerbated by the fact that many additives, such as KI, PEAI, and $Pb(SCN)_2$, passivate defects and stabilize wide-band-gap perovskites.[36–38] Whereas additives are routinely incorporated into solution-processed perovskites by adding a few to hundreds parts-per-million to the perovskite precursors,[36] this is difficult to replicate with thermal evaporation.

A different approach is to shrink the pyramid size and elongate the perovskite charge-carrier diffusion length. In this case, a perovskite layer with a thickness greater than the pyramid height need not be conformal and it can be deposited from solution. There is precedence for this approach: Ju et al. and Nguyen et al. have reported a silicon texturing process with pyramids smaller than 2 μm,[39,40] and several scalable solution-processing approaches that have been reported for single-junction perovskite solar cells[41]—including blade coating,[42,43] slot die coating,[44,45] and spray coating,[46,47]—may conceivably be adapted to this tandem application.

Here we report high-throughput blade coating of a wide-bandgap perovskite on sub-micrometer-scale, double-side-textured silicon to achieve efficient perovskite/silicon monolithic tandem solar cells. In this new tandem device structure, the perovskite cell "planarizes" the textured silicon surface by filling the valleys between pyramids. The texture results in an elongated light path length in the silicon, boosting the bottom cell current compared to a cell with a planar front surface. The tandems

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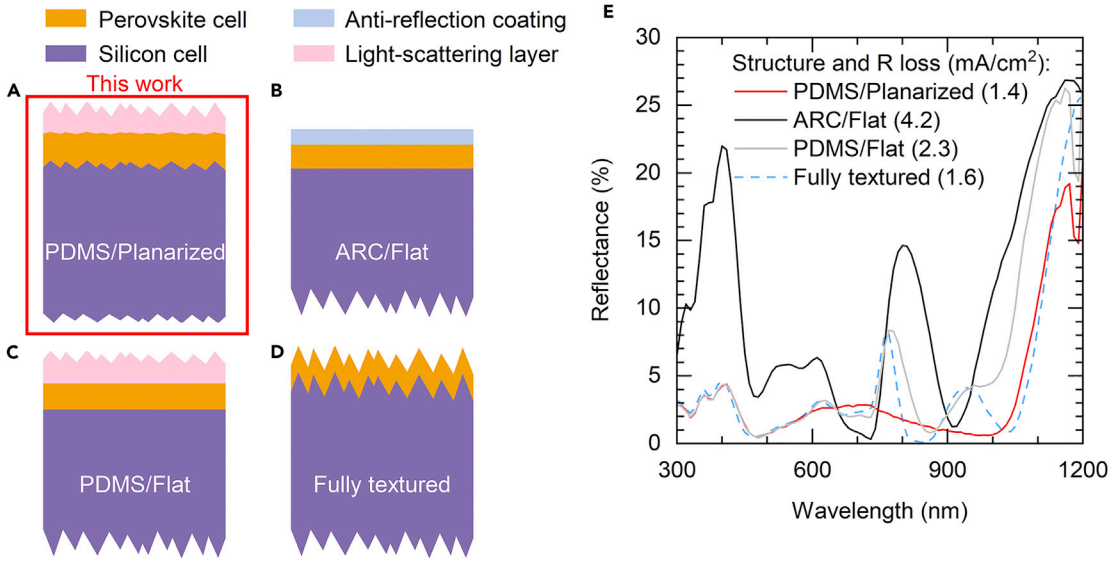

Figure 1. Schematics of Simulated Perovskite/Silicon Tandem Architectures

(A) Double-side textured silicon cell with a planarizing perovskite top cell and a PDMS light-scattering layer.

(B) Front-side-polished silicon cell with a planar perovskite top cell and anti-reflection coating.

(C) Front-side-polished silicon cell with a planar perovskite top cell and PDMS light-scattering layer.

(D) Double-side textured silicon cell with a conformal perovskite top cell.

(E) Simulated reflectance spectra of the tandem architectures and AM1.5G-weighted reflectance (R) loss expressed as a current density.

are finished with a textured front PDMS layer that is representative of textured module glass and that reduces reflectance at the near-planar surface of the perovskite top cell. The resulting "PDMS/Planarized" tandem cells provide a pathway to high matched current densities without costly polishing processes for the silicon bottom cells and with all of the advantages of scalable solution coating methods for the perovskite top cells.

RESULTS AND DISCUSSION

We first investigated the proposed PDMS/Planarized tandem architecture's potential to minimize reflection. To do so, we performed optical simulations with PV Lighthouse's SunSolve software on four different perovskite/silicon tandem configurations, as shown in Figures 1A–1D: a PDMS/Planarized tandem with the PDMS carrying random pyramids reproduced from a textured silicon wafer,[48] a tandem with a polished silicon front surface and an anti-reflection coating on the perovskite cell ("ARC/Flat"), a tandem with a polished silicon front surface and the same textured PDMS light-scattering layer ("PDMS/Flat"), and a tandem with a fully textured silicon bottom cell with a conformal perovskite top cell ("Fully textured"). Following the procedure published by Manzoor et al.,[48] we first built a model to reproduce our previous 25.4%-efficient tandem cell,[8] which featured the ARC/Flat configuration with a silicon heterojunction cell, a triple-cation perovskite cell, and a MgF_2 anti-reflection layer. (The full layer stack and thicknesses can be found in Table S1.) The calculated total absorptance (1-reflectance) and external quantum efficiency (EQE) agree well with the published measured results, as shown in Figure S1, validating our model. We subsequently simulated the remaining configurations in Figure 1 by varying the surface morphology (and light-scattering layer, as appropriate) while keeping the component layers of both sub-cells the same. Note that SunSolve combines a thin-film optical simulator with Monte-Carlo-based ray-tracing and has built-in models for random pyramids with adjustable heights

and angles.[49] The pyramid size on both surfaces of the silicon cell in Figure 1A was 800 nm, and the pyramid size on the other textured surfaces was 3 μm.

The results of the optical simulations appear in Figure 1E. First, replacing the MgF_2 layer in a Flat tandem with a PDMS layer reduces the reflection loss by almost 2 mA/cm^2 because of the "double-bounce" effect introduced by the steep surface texture. This improvement agrees well with the experimental results reported by Bush et al. and Jost et al.[9,10] Second, the Fully textured configuration in Figure 1C further reduces the reflection loss to 1.6 mA/cm^2, which agrees with the value reported by Sahli et al.[25] Third, the PDMS/Planarized tandem produces a reflectance curve similar to that of the Fully textured tandem, with a reflection loss of only 1.4 mA/cm^2. The difference in the spectra in the 700–1000 nm range comes from the fact that the planarizing perovskite layer in the PDMS/Planarized tandem is treated as incoherent in the simulation, whereas the conformal perovskite layer in the Fully textured tandem is treated as coherent. The coherency results in interference fringes because the recombination layer in these simulations (and our previous 25.4%-efficient cell) is indium tin oxide (ITO), which has a relatively low refractive index (2.0 at 600 nm) that causes reflection at the interface between the sub-cells. A higher-refractive-index recombination layer, like the nc-Si:H used experimentally by Sahli et al. to replace ITO,[25] or a lower-refractive-index electron contact of the silicon bottom cell, like the nc-SiO_x:H used by Jošt et al. and Santbergen et al. to replace the a-Si:H,[10,11,50] would suppress this interference and bring the reflectance spectra of the Fully textured and PDMS/Planarized tandems even closer together (Figure S2). Of course, the degree to which light will remain coherent in each of the structures will be determined by the roughness of the perovskite layer and thus its deposition process,[9] but, this uncertainty aside, the simulations reveal that the PMDS/Planarized architecture can have optical performance comparable to that of a Fully textured tandem.

One assumption underpinning the simulations in Figure 1—stemming from the ray tracing in SunSolve—is that sub-micrometer pyramids will have the same reflectance as standard larger pyramids. To realize sub-micrometer pyramids and test this hypothesis, four different potassium-hydroxide-based etching recipes were developed (details in Table S2). Recipe A—our starting baseline texturing recipe—produced the largest pyramids, as revealed by the scanning electron microscopy (SEM) images in Figure 2. The pyramid heights, obtained from atomic force microscopy (AFM), range from 0.43 to 2.5 μm, with a mean of 1.3 μm. The bare wafer textured with Recipe A has an AM1.5G-weighted reflectance (700–1100 nm, the wavelengths seen by the silicon in a tandem) of 11.5%, much lower than the planar wafer in Figure 2, which has 34.4% reflectance. Note that a low measured reflectance for a bare wafer will similarly translate into low reflectance at the perovskite cell/silicon cell interface in a tandem, as the reflectance reduction is caused by the "downward" bouncing of light off pyramid faces regardless of the incident medium. A low reflectance is typically also emblematic of path-length enhancement of weakly absorbed long-wavelength light within the wafer, which will persist in tandem structures.[51] However, with a maximum pyramid height of 2.5 μm, this wafer would require an unreasonably thick perovskite cell to successfully cover the pyramids and suppress shunts. By increasing the ALKA-TEX additive in the texturing solution (Recipe B), the pyramids shrank to a mean height of 0.55 μm with a tighter distribution. With additional potassium silicate, inspired by the work of Ju et al.,[39] Recipe C further reduced the mean pyramid height to 0.43 μm with a maximum height of 0.83 μm. Diminishing the size of the pyramids moderately increased the reflectance of the wafers to 13.1% and 14.2% for Recipes B and C, respectively. Reducing the

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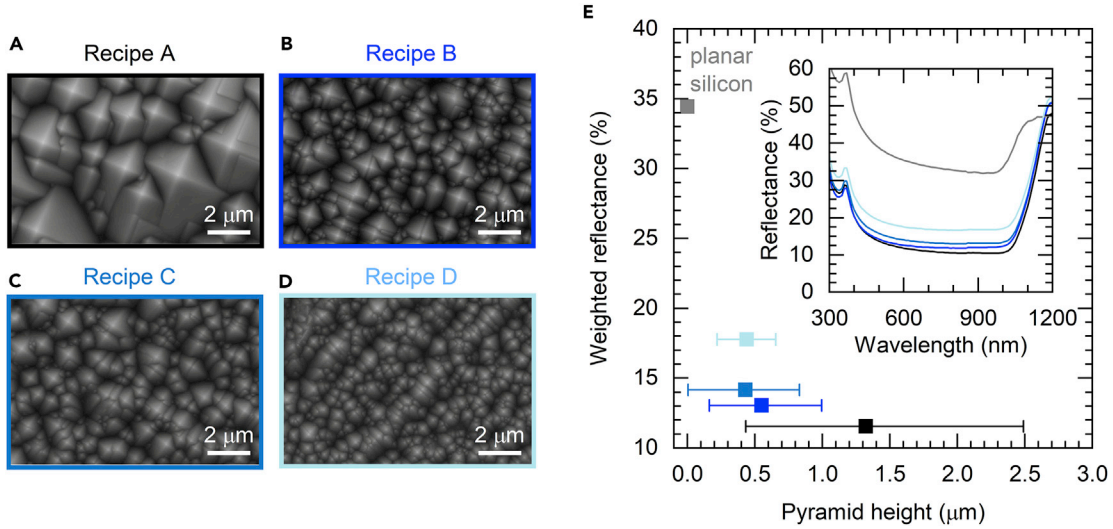

Figure 2. Silicon Wafers with Sub-micrometer Pyramidal Texture

(A–D) Top-view SEM images of silicon wafers textured with different recipes: (A) Recipe A, (B) Recipe B, (C) Recipe C, and (D) Recipe D.

(E) AM1.5G-weighted (700–1100 nm) reflectance and pyramid height distribution (extracted from AFM) of the aforementioned wafers and a reference planar wafer. The inset shows the measured reflectance spectra.

etching time from Recipe C, Recipe D produced a more uniform size distribution with pyramid heights between 0.23 and 0.66 μm, but the reflectance jumped significantly to 17.8%.

Angle-resolved reflectance measurements, presented in Figure S3, explain the data in Figure 2E: large pyramids (Recipe A) reflect normally incident light primarily at an angle of 20° off incidence, whereas smaller pyramids (Recipe D) shift the primary reflection to 17° off incidence. Based on the geometry of the pyramids,[49] this change corresponds to a decrease in pyramid base angle from 50° to 49°, which was shown by Baker-Finch et al. to result in higher hemispherical reflectance.[49] Moreover, the angle-resolved reflectance curves become broader for smaller pyramids. This broadening could be due to diffractive effects happening at the edges and peaks of the pyramids, as found by Haug et al. and Yang et al.,[52,53] which would increase the reflectance. Furthermore, for Recipes B–D, a portion of the pyramids are smaller than 300 nm and thus break the geometrical optics limit identified by Llopis et al.[54] Beyond this limit, transmitted light is not tilted with respect to the normal of the macroscopic wafer surface, and it therefore no longer experiences two bounces. Balancing the trade-off between small pyramids for subsequent perovskite coating and increasing reflectance, we chose Recipe C for the rest of the tandem development.

To test the ability of a perovskite top cell to planarize the sub-micrometer-textured wafers, we applied a nitrogen (N_2)-knife-assisted blading process[55] to coat the poly [bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) hole-transport layer and perovskite layer. As illustrated in Figure 3A, a N_2 knife helps remove solvent vapor, facilitating a quick transition of solution into solid during the blading process. Whereas the perovskite layer can be thick and planarizing in our new tandem cell design, the PTAA layer must still be thin, uniform, and thus conformal to the pyramids because PTAA impedes hole transport when it is thicker than approximately 15 nm, reducing cell fill factor (Figure S4).[56,57] As shown in Figure 3B, spin coating 2 mg/mL PTAA in toluene at 5,000 rpm for 30 s on a silicon bottom cell creates a non-uniform layer with

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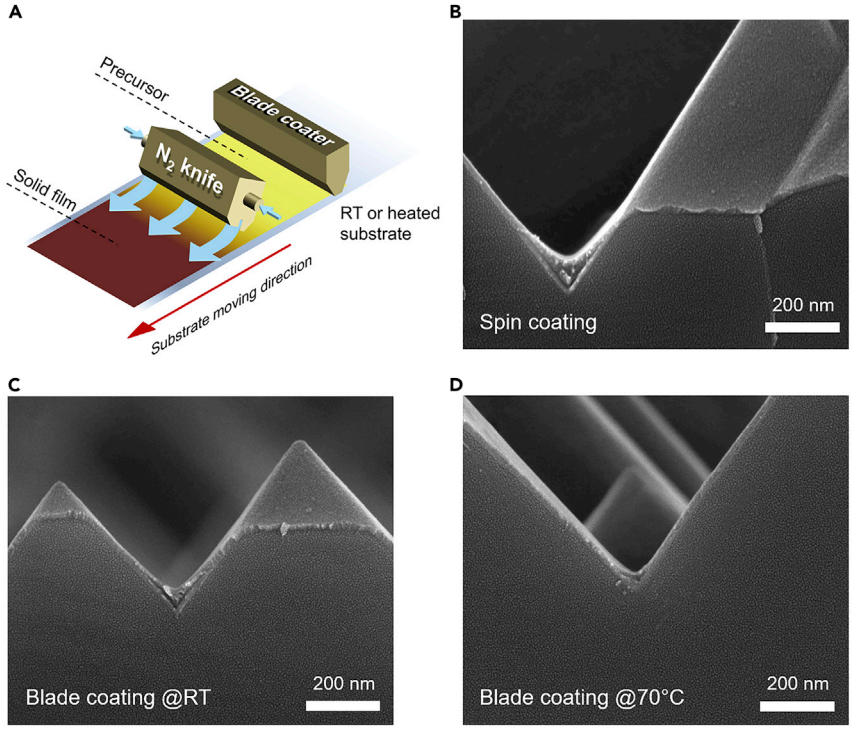

Figure 3. Blade Coating PTAA Layers on Textured Silicon Bottom Cells

(A) Illustration of N_2-assisted blade coating.

(B–D) SEM images of PTAA on textured silicon bottom cells deposited by (B) spin coating, (C) N_2-assisted blade coating with the substrate at room temperature (RT), and (D) N_2-assisted blade coating with the substrate at 70°C. The three layers that are visible are the silicon wafer, ITO front electrode of the silicon cell, and PTAA hole-transport layer.

a thickness of 8 nm on the pyramids facets but up to 45 nm in the valleys. Similarly, blade coating PTAA at room temperature results in a non-uniform layer, even with N_2-assisted drying (Figure 3C). However, elevating the substrate temperature to 70°C during blade coating produces the desired thin, uniform PTAA layer on the textured silicon surface (Figures 3D and S5), which we ascribe to accelerated evaporation of the solvent.

The perovskite layer coated on top of the PTAA must be thick enough to bury the underlying pyramids—protruding pyramids will shunt the top cell—while still thin enough to collect photogenerated carriers. As the carrier diffusion length in these perovskites is on the order of 1 μm,[58] this means that the perovskite layer should preferably be <2 μm thick (and no large outlier pyramids can be tolerated). Fortunately, as shown in Figure S6, the thickness of a blade-coated perovskite layer can be tuned through the concentration of the perovskite precursor, gap distance between the blade and substrate, and blade-coating speed. An additional challenge is to produce dense films at these thicknesses that are in intimate contact with the textured silicon surface: Figure 4 reveals voids near the pyramid valleys with unoptimized perovskite solutions. We found that this problem can be eliminated through solvent engineering designed to balance solution drying and perovskite grain growth. In particular, for 1.55 M $Cs_{0.1}MA_{0.9}Pb(I_{0.9}Br_{0.1})_3$ perovskite precursor in 2-methoxyethanol (2-ME) with 0.05 mol% ratio of surfactant L-α-phosphatidylcholine (LP) to Pb, we tuned the ratio of DMSO/Pb in precursor from 0 to 50 mol% because DMSO coordinates with the perovskite and is thus expected to change

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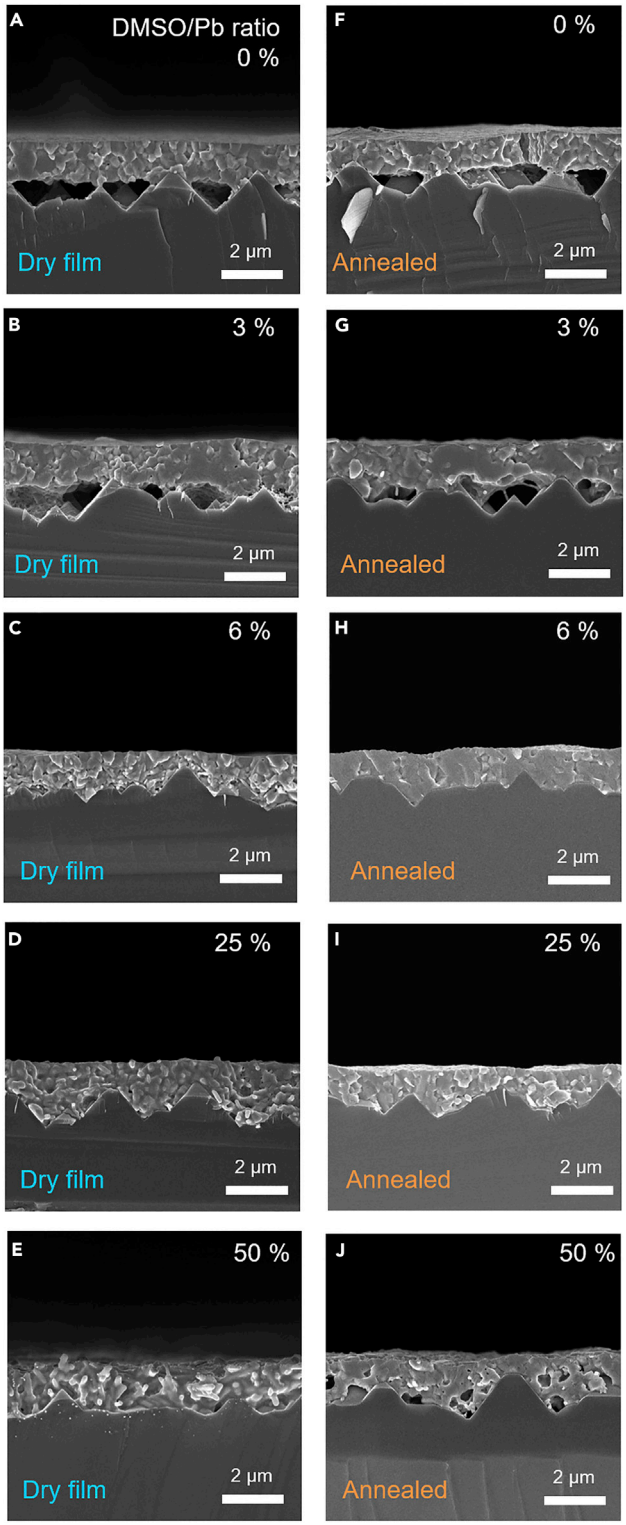

Figure 4. Impact of DMSO on the Filling of Perovskites on Textured Silicon Wafers during the Drying and Annealing Processes

(A–J) SEM images of films made by blade coating $Cs_{0.1}MA_{0.9}Pb(I_{0.9}Br_{0.1})_3$ precursor with 0.05 mol% LP and different DMSO/Pb ratios: (A) 0 mol%, (B) 3 mol%, (C) 6 mol%, (D) 25 mol%, and (E) 50 mol% before annealing and (F) 0 mol%, (G) 3 mol%, (H) 6 mol%, (I) 25 mol%, and (J) 50 mol% after annealing at 70°C for 10 min and 100°C for 15 min.

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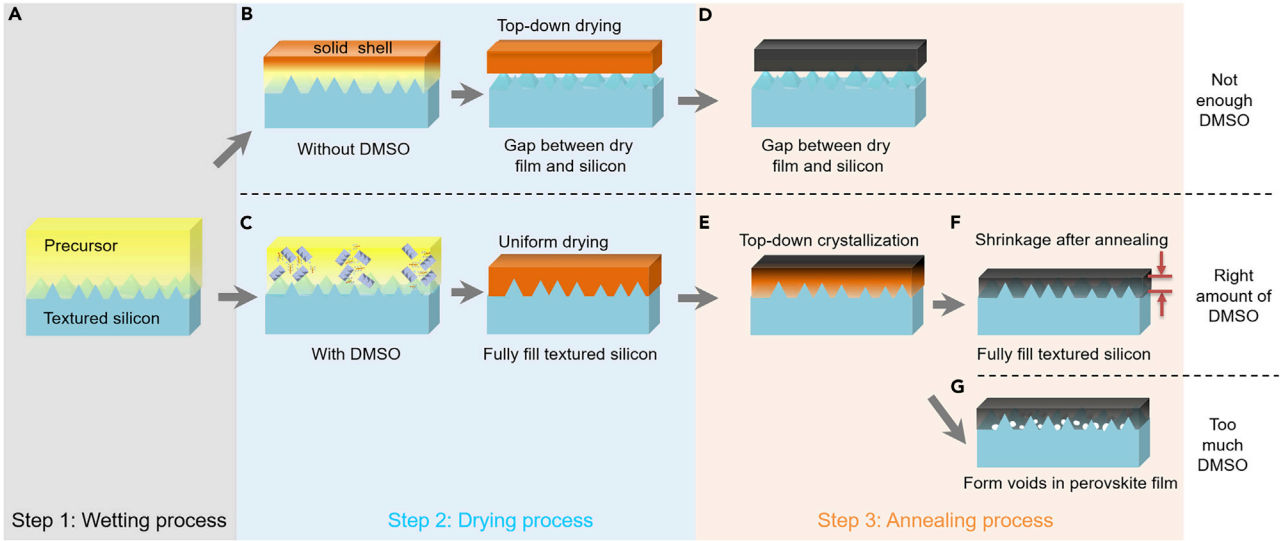

Figure 5. Mechanism of Dense Perovskite Film Formation

(A–G) Schematic depiction of the evolution of a perovskite layer on a textured surface during (A) wetting, (B) drying without DMSO or (C) with DMSO, and (D–G) annealing with different amounts of DMSO: (D) not enough DMSO, (E) top-down crystallization with DMSO, (F) right amount of DMSO, and (G) too much DMSO.

the drying and crystallization processes. For solid-state perovskite films after drying and before annealing (referred to hereafter as dry films), void-free coverage of the textured wafer occurs for DMSO/Pb ratios between 6 and 50 mol% (Figures 4C–4E). Conversely, there is an extended void between the dry film and wafer for DMSO/Pb ratios of 3 mol% or less (Figures 4A and 4B). After annealing at 70°C for 10 min and 100°C for 15 min, the perovskite film remains dense for DMSO/Pb ratios of 6–25 mol% (Figures 4H and 4I), but voids appear at the bottom of and inside the annealed film with a DMSO/Pb ratio of 50 mol% (Figure 4J). We note that the surfactant LP in the perovskite precursor also facilitates the formation of void-free dry films on the textured surfaces, as shown in Figure S7, by suppressing the Marangoni solution flow inside wet films.[43]

The best additive concentration (25 mol% DMSO, Figures 4D and 4I) enables a dense $Cs_{0.1}MA_{0.9}Pb(I_{0.9}Br_{0.1})_3$ film to be blade coated from a low-boiling-point solvent (2-ME) at a speed of 25 mm/s or 1.5 m/min. Both the dry and annealed films are dense and fully cover the textured wafer, with a thickness of approximately 1.5 μm from the bottom of the pyramids. Bladed perovskite films on textured wafers and on flat reference wafers show nearly the same photoluminescence intensities and charge-carrier recombination lifetimes (Figure S8), indicating their high quality. Furthermore, we found that this engineered perovskite solution works not only for blade coating but also for spin coating of films onto sub-micrometer-textured silicon. Figures S9–S11 show dense $Cs_{0.1}MA_{0.9}Pb(I_{0.9}Br_{0.1})_3$ and $FA_{0.85}MA_{0.15}Pb(I_{0.85}Br_{0.15})_3$ perovskite films spun onto textured wafers.

To understand how the dense perovskite films form on the textured wafers, we decoupled the process into three steps, illustrated in Figure 5: wet film formation by blade coating, film drying by N_2-blowing, and film crystallization by annealing. During blade coating, a layer of perovskite solution is transferred onto the substrate. The solvent is primarily 2-ME with a small amount of DMSO, where 2-ME is highly volatile but non-coordinating with the perovskite material,[55,59] and DMSO is non-volatile but can coordinate with the perovskite material to form an intermediate

phase.[23] During N_2-blowing, 2-ME quickly volatilizes, leaving dry films coordinated with DMSO. Due to the limited amount of DMSO, the dry films are often a mixture of perovskite and perovskite-DMSO intermediate phase, as shown in the X-ray diffraction (XRD) patterns in Figure S12. Subsequent annealing converts the intermediate phases to perovskite, accompanied by grain growth. To investigate whether the extended voids between the dry films and textured wafers in Figures 4A and 4B are formed during wetting or drying, we froze a sample right after blading the perovskite solution and examined it under cryo scanning electron microscopy (cryo-SEM). As shown in Figure S13, DMSO-free perovskite solution fully fills the pyramid valleys, revealing that it is the drying process that causes void formation. Drying starts at the solution/air interface as the solvent at the top surface evaporates, quickly forming a solid top shell. The solid film then grows from the shell downward as the remaining solution dries, leaving voids when the last 2-ME solvent evaporates and no perovskite precursor remains to fill its volume, as illustrated in Figure 5B. For solutions with DMSO, the quick formation of a top solid shell is prohibited by its high boiling point and strong chemical coordination with the perovskite (Figure 5C). That is, the perovskite-DMSO intermediate-phase particles interrupt shell formation and allow 2-ME solvent to evaporate, suppressing the void formation.

However, when the perovskite solution has too much DMSO, the dry film still fully fills the pyramid valleys, but annealing causes voids to form, as shown in Figures 4E and 4J. This can be explained by the shrinkage of the dry film upon annealing due to the removal of DMSO from the intermediate phase. To illustrate this, we measured the thickness of a perovskite film coated from a precursor with a DMSO/Pb ratio of 25 mol% onto a PTAA-coated ITO/glass substrate (Figure S14A). The thickness decreased by 13% after annealing, and films with other DMSO concentrations similarly shrank in proportion to their concentrations (Figure S14B). As with the drying of films with too little DMSO, the annealing-induced crystallization of films with too much DMSO proceeds from the top surface downward and produces voids when the last solvent—in this case, DMSO instead of 2-ME—leaves. Only for moderate and small DMSO concentrations ($\leq$25% in this experiment) can the volume reduction upon DMSO departure be compensated by perovskite diffusion, thus maintaining a dense perovskite film on textured silicon after annealing.

The best condition for a dense perovskite absorber layer on textured silicon is thus N_2-assisted blade coating at room temperature, followed by thermal annealing for perovskite crystallization. While it is tempting to try combining the drying and crystallization processes by blade coating the perovskite film on a hot substrate with a N_2 knife, we found that this again generates voids between the perovskite film and textured silicon substrate after blading (Figure S15). Similar to the case illustrated in Figure 5B, this is because the hot substrate accelerates the drying of the perovskite precursor, which forms a solid shell on the top of the film and create voids at the bottom.

After successfully planarizing a textured silicon bottom cell with a dense perovskite absorber layer, we completed tandem devices with 30-nm-thick C_{60}, 9-nm-thick tin oxide (SnO_2), and 60-nm-thick ITO layers, as well as a 500-nm-thick silver front electrode, deposited by thermal evaporation, atomic layer deposition, sputtering, and thermal evaporation, respectively. Finally, the tandem device was capped with a textured PDMS light-scattering layer to reduce the reflection loss at the planarized front surface, as shown in Figures 6A and S16. The SEM cross-section (without the PDMS layer) in Figure 6B clearly shows that the perovskite top cell fully buried and

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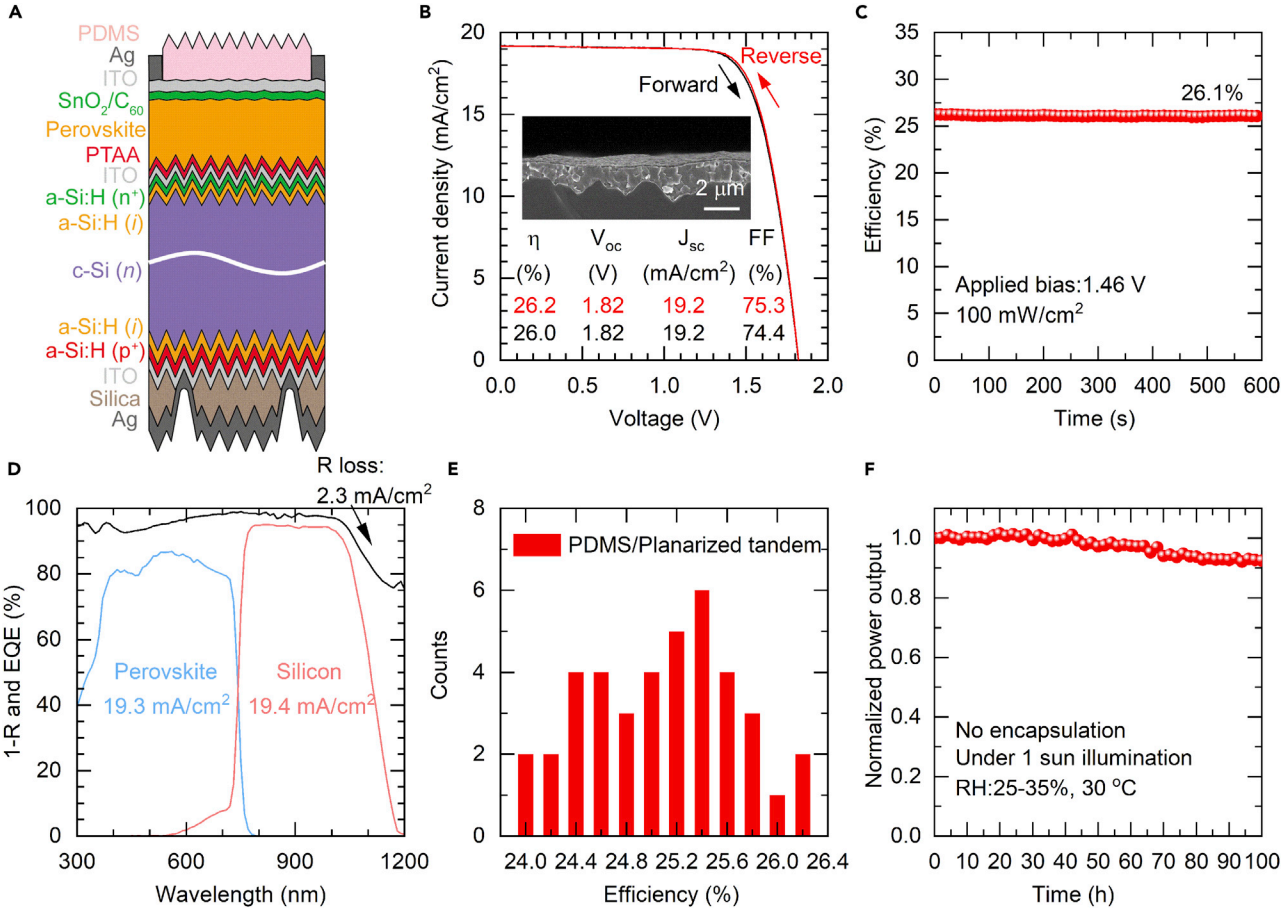

Figure 6. Perovskite/Silicon Tandem Solar Cell Performance

(A) Schematic illustration of a PDMS/Planarized perovskite/silicon tandem solar cell.

(B) *J–V* curves of the champion PDMS/Planarized tandem solar cell under reverse scan and forward scan, and SEM cross-section of a perovskite top cell planarizing a textured silicon cell (inset).

(C) Steady-state output of the champion cell at the maximum power point under simulated AM1.5G illumination.

(D) EQE and total absorptance (1-R, where R is the reflectance) of the champion cell.

(E) Efficiency distribution for 40 PDMS/Planarized tandem solar cells.

(F) Stability of an unencapsulated PDMS/Planarized tandem cell under simulated AM1.5G illumination in ambient atmosphere.

planarized the sub-micrometer-textured silicon bottom cell. Figure 6B plots the current-voltage (*J–V*) characteristic of the champion perovskite/silicon tandem device under reverse scan and forward scan, for which the power conversion efficiency is 26.2% and 26.0%, respectively, with very small *J–V* hysteresis. For comparison, the performance of the constituent single-junction perovskite top cells and silicon bottom cells is shown in Figures S17–S19. The champion tandem was held at its maximum power point for 600 s and maintained a stabilized power conversion efficiency of 26.1% (Figure 6C), which agrees with the efficiency values obtained from the *J–V* curves. The EQE spectra in Figure 6D reveal the matched current density between the sub-cells in the PDMS/Planarized tandem, and Figure S20 shows that this current density is 1.7 mA/cm^2 higher than that of the limiting sub-cell when the PDMS light-scattering layer is omitted. The PDMS/Planarized tandem showed the same J_{SC} values under simulated AM1.5G illumination without or with additional blue (or IR) light, which confirmed the matched current density of the sub-cells. The performance statistics of 40 PDMS/Planarized tandem cells demonstrate that blade coating the perovskite top cells onto textured silicon bottom cells is as reproducible

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as spin-coating perovskite top cells onto flat silicon bottom cells (Figures 6E and S21), which we reported previously.[8] The unencapsulated PDMS/Planarized tandem cell maintained 92% of its initial efficiency after constant illumination for 100 h in ambient atmosphere (Figure 6F).

As revealed by the 1-reflectance curve in Figure 6D, the current loss from reflection for this PDMS/Planarized tandem cell is 2.3 mA/cm^2, which approaches the 1.6 mA/cm^2 loss reported by Sahli et al. for a fully textured perovskite/silicon tandem fabricated by vacuum deposition.[25] For comparison, a reference PDMS/Flat perovskite/silicon tandem device (Figures S22 and S23) had a larger reflection loss of 3.3 mA/cm^2, which is similar to that of the PDMS/Flat tandem reported by Bush et al.[9] This 1 mA/cm^2 current gain is in agreement with the simulations in Figure 1, validating the current advantage of the new tandem architecture. Note that the absolute reflectance value for the PDMS/Planarized cell is slightly higher than the simulated value, and the comparison between the measured and simulated reflectance spectra in Figures S24 and S25 reveals that the measured data have a constant offset of 1%–2%. This is consistent with reflectance from the silver fingers, which are not included in the simulation and are wavelength independent; although we tried to focus the incident beam between fingers when measuring the reflectance, the PDMS light-scattering layer makes it impossible to not have some contribution from the fingers. As predicted by the simulations in Figure 1, the PDMS/Planarized tandem cell has a near-constant low reflectance from 750 to 1,050 nm due to the elimination of interference fringes, resulting in a near-constant EQE of 95% in that wavelength range (Figure 6D). The main current loss mechanism in this device is parasitic absorption, especially in the front electron transport and transparent conductive oxide layers of the perovskite top cell, as evident from the large gap between the 1-reflectance and EQE curves between 300 and 600 nm (Figure 6D). When the parasitic absorption is eliminated, the summed J_{sc} from both sub-cells would increase by 1.6 mA/cm^2, from 38.7 mA/cm^2 to 40.3 mA/cm^2.

Conclusions

We demonstrated a new perovskite/silicon tandem solar cell architecture with the manufacturing potential of a solution-deposited top cell and the performance potential of a vapor-deposited conformal top cell. Consistent with present commercial processes, the silicon bottom cell was fully textured with scalable chemistries, which were tuned to ensure all pyramids were smaller than 1 μm. The sub-micrometer pyramids and precursor additives enabled solution-processed dense perovskite layers that fully cover the silicon texture. The perovskite layer was blade coated in ambient atmosphere at a speed of 1.5 m/min, which corresponds to more than 1 wafer per second for an industrial blade coater with a width of 1 m. This work focused on the current density of this new tandem device architecture, extending the path length of long-wavelength light within the silicon and reducing the reflection loss to 2.3 mA/cm^2 to reach a matched J_{sc} above 19 mA/cm^2 and an efficiency of 26%. However, there remain tangible opportunities to, for example, boost *FF* by 10% by reducing the full-stack contact resistances of the top-cell contacts, augment V_{oc} by at least 0.15 V through defect passivation of bladed perovskite films, and even further increase J_{SC} by 1 mA/cm^2 by minimizing the parasitic absorption. That is, there is no fundamental barrier to exceeding 30% efficiency with this device design and fabrication process. We thus expect that this tandem architecture is poised to be adopted by silicon solar cell manufacturers that are hunting for tandem technologies with low required capital expenditures, the potential for rapid scaling, and minimum modification of their silicon cells.

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EXPERIMENTAL PROCEDURES

Materials

Methylammonium iodide and methylammonium bromide were purchased from Greatcell Solar company. PbI_2 (99.999%), $PbBr_2$ (99.999%), CsI (99.999%), N,N-dimethylformamide (99.8%, anhydrous), 2-methoxyethanol (99.8%, anhydrous), dimethyl sulfoxide (99.8%, anhydrous), and poly(triaryl amine) were purchased from Sigma-Aldrich. C60 was purchased from NANO-C company.

Silicon Solar Cell Fabrication

Silicon wafers were textured in potassium-hydroxide-based solutions, per the details in Table S2. The wafers were then cleaned in piranha, RCA-B, and buffered oxide etchant solutions prior to deposition of amorphous silicon (a-Si:H) layers. Intrinsic and p-type a-Si:H films (6 and 15 nm thick, respectively) were first deposited by plasma-enhanced chemical vapor deposition on the rear side of the wafer, and intrinsic and n-type a-Si:H films (6 and 8 nm thick, respectively) were then deposited on the front side. Detailed plasma-enhanced chemical vapor deposition processes are published elsewhere.[60] A 20-nm-thick ITO layer was sputtered from a 90/10 In_2O_3/SnO_2 target in an MRC 944 tool on the front side of the wafer through a shadow mask to define 7 × 7 mm square cells. A 20-nm-thick ITO layer was also sputtered on the textured rear surface through the same shadow mask, followed by a 300-nm-thick silica layer spray coated through a stainless-steel mesh to define local contact openings, and finally, a 200-nm-thick sputtered silver layer. The silicon cells were then annealed at 200°C for 20 min before fabricating perovskite cells on top. The silicon wafer was laser scribed into 16 × 16 mm square chips with one silicon solar cell on each chip.

Perovskite/Silicon Tandem Solar Cell Fabrication

The PTAA layer was coated on the ozone-plasma-treated silicon bottom cell by N_2-assisted blade coating at 25 mm/s with a substrate temperature of 50°C–70°C in ambient conditions. The N_2 knife worked at 10.0 psi, and the blade-to-substrate gap was 100 μm. PTAA layer was annealed at 70°C for 10 min in ambient atmosphere. The perovskite film was prepared by blade coating $Cs_{0.1}MA_{0.9}Pb(I_{0.9}Br_{0.1})_3$ precursor in ambient conditions. The $Cs_{0.1}MA_{0.9}Pb(I_{0.9}Br_{0.1})_3$ precursor was 1.55 M in 2-ME with 25 mol% of DMSO, 0.05 mol% of LP/Pb, and 0.1 mol% of MAH_2PO_2/Pb. The blade-coating speed was 25 mm/s, the blade-to-substrate gap was 200 μm, and the N_2 knife worked at 20.0 psi. After N_2-assisted blade coating, the perovskite films were annealed at 70°C for 10 min and 100°C for 15 min in ambient atmosphere with relative humidity less than 35%. Next, we thermally evaporated 30 nm of C_{60} at a deposition rate of 0.15 Å/s. Then, 9 nm SnO_2 was deposited in a CambridgeNanoTech Savannah G2 tool with the following processing sequence for 55 cycles: 0.5 s TDMASn pulse, 15 s purge (20 sccm N_2), 0.1 s deionized water pulse, and 15 s purge (20 sccm N_2). During SnO_2 deposition, the substrate temperature was maintained at 100°C, and the TDMASn and water precursor temperatures were maintained at 60°C and room temperature, respectively, while the valve manifold, exhaust line, and trap temperatures were maintained at 150°C, 130°C, and 150°C, respectively. 60 nm of ITO was sputtered from a 4-inch ITO target with 100 W power in a Kurt J. Lesker PVD 75 Pro Line tool on top of the SnO_2, through a shadow mask to define 6.5 × 6.5 mm square cells. Three Ag fingers with a width of 130 μm, length of 6.5 mm (the full width of the cells), and thickness of 500 nm were thermally evaporated on top of the ITO layer. A PDMS light-scattering layer with the negative of a silicon wafer's random pyramid texture (2–5 μm pyramid size) was made with Sylgard 184 from Dow Corning, where the base and curing agent

were mixed in a 10:1 ratio and then further diluted with toluene in a 10:1 weight ratio. After degassing, the PDMS precursor was dispensed onto the silicon wafer and cured at 46°C for 12 h before being carefully separated from the wafer by hand. Finally, the PDMS light-scattering layer was carefully placed onto the perovskite/silicon tandem device to avoid any trapped air between the PDMS and device. The attachment was thus via Van der Waals forces, without index-matching liquid.

Device Characterization

Current-voltage measurements were recorded using a Keithley 2400 Source-Measure Unit under simulated AM1.5G irradiation (100 mW cm^{-2}), which was produced by a Xenon-lamp-based solar simulator (94043A, Newport Sol3A Class AAA). The light intensity was calibrated using a 91150-KG5 silicon reference cell and meter with a KG5 window. The voltage scan rate was 0.1 $V \cdot s^{-1}$. The *J–V* curves were measured without light soaking or electric-poling preconditioning. XRD measurements were performed with a Rigaku D/Max-B X-ray diffractometer with Bragg-Brentano parafocusing geometry, a diffracted-beam monochromator, and a conventional cobalt target X-ray tube set to 40 kV and 30 mA. Scanning electron micrographs were taken with a FEI Helios 600 Nanolab and SEM-FEG XL30. The PL spectrum and TRPL were measured by a PicoQuant Flue Time 300 instrument at room temperature. The excitation source was a 482 nm pulsed laser. The laser excitation power for the spectral PL measurement was 18 mW cm^{-2} at a repetition frequency of 10 MHz. TRPL data were measured with a laser excitation power of 1.9 nW cm^{-2} per pulse at a repetition frequency of 0.2 MHz. EQE spectra were measured using a PV Measurements QE-X10 tool. When measuring perovskite top cells, the tandems were light-biased by a white light equipped with a long-pass (>800 nm) filter; when measuring silicon bottom cells, the tandems were light-biased by a green LED. The hemispherical reflectance was measured at a 7° angle of incidence using a PerkinElmer Lambda 950 spectrophotometer equipped with an integrating sphere, whereas the angular-resolved reflectance was measured with the same spectrophotometer but equipped with an Automated Reflectance/Transmittance Analyzer (ARTA) accessory.[61]

SUPPLEMENTAL INFORMATION

Supplemental Information can be found online at https://doi.org/10.1016/j.joule.2020.01.008.

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AUTHOR CONTRIBUTIONS

J.H., Z.C.H., B.C., and Z.J.Y. conceived the idea. B.C. fabricated the top cell and completed the tandem device. Z.J.Y. performed the optical simulation and developed the texturing recipes. S.M. performed optical characterization of the textured wafer and tandem devices. Z.J.Y. and W.W. fabricated the silicon bottom cells. B.C., G.Y., Z.Y., and X.D. led the efforts on developing the perovskite top cells. S.W. carried out cryo-SEM measurement. Z.N. conducted the PL and TRPL measurements. B.C. performed SEM measurement. B.C., Z.J.Y., Z.C.H., and J.H. wrote the paper.

DECLARATION OF INTERESTS

Z.J.Y., Z.C.H., J.H., and B.C. are inventors on a patent application filed August 12, 2019 related to this work.

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